AMENDMENTS TO THE SPECIFICATION

Each paragraph or section to be amended is indicated by presentation herebelow of a replacement paragraph or section marked up to show changes made relative to the immediate prior version.

Please replace paragraph [0003] with the following re-written paragraph:

[0003] As a result, circuit package design typically has depended upon integrated circuit design to solve the problems presented by high frequency signal propagation. For example, United States patent number 6,115,298 to Kwon et al. discloses a semiconductor device ~~to~~ that includes a circuit to reduce impedance mismatch between the semiconductor device and a bus connected thereto. The bus consists of a plurality of signal lines. The semiconductor device includes a discrete resistor, corresponding to the impedance of the signal lines. The signal lines are connected to a plurality of second pads. A reference voltage generator generates a reference voltage. A comparator compares a voltage on the first pad with the reference voltage, generating a control signal in response to the comparison. A code generator generates a code signal in accordance with the control signal to produce a current on the first pad. A data driver drives data signals to the code signal, thereby matching the impedance of the data driver with the impedance of the signal lines.

Please replace paragraph [0004] with the following:

[0004] United States patent number 5,808,478 to Andresen discloses a buffer with a slew rate that is load independent. The buffer is comprised of an output buffer connected to an output terminal. The output buffer is controlled such that it can drive a load with different drive levels by changing the transconductance internal thereto. The transition on the input to the buffer is passed through an intrinsic delay block to provide a delay signal on a node. A first phase detector latch with a first threshold voltage compares this transition with the transition on the output terminal. A second phase detector latch with a second threshold voltage, also compares this delayed transition with that on the output terminal. If both of the latches indicate that the delayed transition occurred after the transition on the output terminal, a control signal on a line is changed by incrementing a counter. This will change the drive to a load. If the transition on the output terminal occurs after the delayed transition, then the counter increments the count value in the opposite direction, increasing the drive to the load to increase the speed of the output driver.

Please replace paragraph [0017] with the following:

[0017] Referring to both Figs. 4 and 5, although the foregoing has been explained with respect to controlling the impedance at output 118, $R_{TOTALDRIVER}$, the same holds true for the impedance at input 116, R_{INPUT}, used as a pull-up and termination voltage resistor.

To that end, a termination resistor Rm_{INPUT} is connected to both input 116 and a power plane at 21f. Termination resistor Rm_{INPUT} is formed by introducing resistive fill in via 25 and has a value selected so that it matches the characteristic impedance, Z_0, of transmission line 114b. This properly terminates a signal arriving at input 116. Additionally, ~~were~~ other inputs or ouputs (I/Os) present on driver 112, shown as I/O 127, may be connected to a resistive via, such as 26, in order to achieve impedance matching between I/O 127 and conductive plane 21e. It should be noted that the value of the resistors defined by filling vias 22, 25 and 26 with resistive material may be controlled by varying the dimensions of the vias, employing resistive fill with differing resistivity or both. As a result a great amount of flexibility is provided with not only matching the impedance between driver I/Os, but also ensuring that the resistivity provided by vias 22, 25 and 26, are identical.